Status of the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (original) A serial data interface system comprising:

a first transceiver configured to comply with a first standard coupled to a set of pins; and

a second transceiver configured to comply with a second standard coupled to the set of pins.

2. (original) The system of claim 1, wherein:

the first standard is IEEE 1394-1995/1394a-2000 standard; and

the second standard is IEEE 1394b-2002 standard.

3. (currently amended) The system of claim 1, wherein the first transceiver device comprises:

a twisted-wire pair (TP) bias section;

a first TP transceiver section; and

a second TP transceiver section.

4. (currently amended) The system of claim 3, wherein the TP bias section comprises:

a TP bias device; and

a connection detection device.

5. (original) The system of claim 3, wherein the first TP transceiver section comprises:

a strobe signal device;

a data signal device;

an arbitration signal device; and

a speed detection device.

6. (original) The system of claim 5, wherein at least one of the strobe signal, data signal, arbitration signal, and speed detection devices is an asynchronous device.

7. (original) The system of claim 3, wherein the second TP transceiver section comprises:

a strobe signal device;

a data signal device;

an arbitration signal device; and

a bias signal detection device.

8. (original) The system of claim 7, wherein at least one of the strobe signal, data signal, arbitration signal, and bias signal detection devices is an asynchronous device.

9. (original) The system of claim 1, wherein the second transceiver comprises:

a transmitter section coupled to the second pin; and

a receiver section coupled to the first pin.

10. (original) The system of claim 9, wherein the transmitter section comprises:

a clock;

a serializer; and

a driver.

11. (currently amended) The system of claim 10, wherein the serializer comprises a N to 1 serializer, wherein N is an integer equal or larger than 2.

12. (original) The system of claim 9, wherein the receiver section comprises:

a clock recovery system;

a deserializer;

a comma detect and alignment device; and

a signal detect device.

13. (original) The system of claim 12, wherein the deserializer comprises a 1-to-N deserializer, wherein N is an integer number equal to or larger than 2.

14. (original) The system of claim 12, wherein the clock recovery system comprises:

a phase detector;

a loop filter; and

a phase interpolator.

15. (original) A serial data interface system, comprising:

a first section configured to comply with a first standard including,

a TPBIAS device section coupled to first and second pins (through additional circuitry),

a first transceiver section coupled to the first and second pins, and

a second transceiver section coupled to the third and fourth pins, and

a second section configured to comply with a second standard including,

a signal transmitting device coupled to the third and fourth pins, and

a signal receiving device coupled to the first and second pins.

16. (original) The system of claim 15, wherein:
the first standard is IEEE 1394-1995/1394a-2000 standard; and
the second standard is IEEE 1394b-2002 standard.

17. (cancelled)

18. (original) A method comprising:
(a) transmitting and receiving data in compliance with a first standard on first and second differential media pairs;
(b) transmitting data in compliance with a second standard on the first differential media pair;
(c) receiving data in compliance with the second standard on the second differential media pair; and
(d) switching use of the first and second differential media pair between step (a) and steps (b) and (c).

19. (original) The method of claim 18, wherein steps (b) and (c) are performed substantially simultaneously.

20. (original) The method of claim of claim 18, further comprising:
using IEEE 1394-1995/1394a-2000 as the first standard; and
using IEEE 1394b-2002 as the second standard.

21. (original) The system of claim 1, wherein the first transceiver comprises:
a bias section;
a first transceiver section; and
a second transceiver section.

22. (original) The system of claim 21, wherein the bias section comprises:
a bias device; and
a connection detection device.

23. (original) The system of claim 21, wherein the second transceiver section comprises:

a strobe signal device;

a data signal device;

an arbitration signal device; and

a bias signal detection device.

24. (original) The system of claim 23, wherein at least one of the strobe signal, data signal, arbitration signal, and bias signal detection devices is an asynchronous device.